

Transient Characteristics and Accommodative Current Limiting Strategy for Bidirectional Interlinking Converters in Hybrid AC/DC Microgrids

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Abstract—Bidirectional interlinking converter (BIC) is the core equipment in a hybrid AC/DC microgrid connected between AC and DC sub-grids. However, the variety of control modes and flexible bidirectional power flow complicate the influence of AC faults on BIC itself and on DC sub-grid, which potentially threaten both converter safety and system reliability. This study first investigates AC fault influence on the BIC and DC bus voltage under different BIC control modes and different pre-fault operation states, by developing a mathematical model and equivalent sequence network. Second, based on the analysis results, a general accommodative current limiting strategy is proposed for BIC without limitations to specific mode or operation condition. Current amplitude is predicted and constrained according to the critical requirements to protect the BIC and relieving the AC fault influence on the DC bus voltage. Compared with conventional methods, potential current limit failure and distortions under asymmetric faults can also be avoided. Finally, experiments verify feasibility of the proposed method.

Index Terms—Bidirectional interlinking converter, current limiting, fault characteristic, hybrid AC/DC microgrid, variation/oscillation of DC bus voltage.

I. INTRODUCTION

DC microgrid is gaining attention for the merits of high-power transmission efficiency, no synchronization problem, and economy. With AC utility grid and AC distributed energy resources (DERs) still occupying dominant position, hybrid AC/DC microgrid possesses a promising future for providing an optimal choice combining AC, DC sub-grids together [1], [2]. As the topology shown in Fig. 1, the AC/DC DERs usually adopt control schemes with droop characteristics to achieve autonomous power sharing without communication [2]. The BIC bridges the AC/DC sub-grids to promote

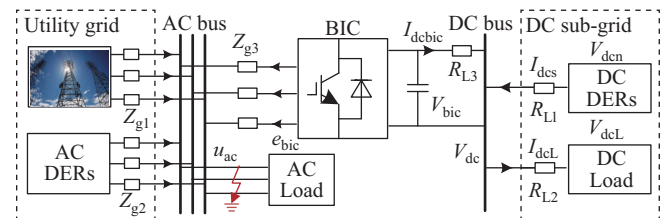


Fig. 1. Topology of a hybrid AC/DC microgrid.

mutual power support and help to maintain the bus stability, whose reliability is significant.

However, when an AC fault occurs, BIC should remain connected [3], which may introduce overcurrent to itself and give rise to severe variation/oscillation of DC bus voltage, threatening the BIC safety and even power supply reliability of DC sub-grid. Furthermore, the variety of control modes (including the DC voltage control, power control and AC voltage control modes [1], [4], [5]) and flexible bidirectional power flow complicates the fault characteristics, as well as different protection requirements. Therefore, it is necessary to figure out fault performance due to the different operational conditions and put forward effective fault ride-through (FRT) strategies.

Great efforts have been devoted by many researchers to investigating the fault characteristics of converters by now. Ref. [6], [7] comprehensively study the fault response of current-controlled and voltage-controlled inverters under symmetric/asymmetric faults. It is disclosed that the inrush current of the later is larger. Further, Ref. [8] analyzes the AC fault influence on BIC based on a modular multilevel converter (MMC) topology at the pre-fault inverter state. However, the DC side of the above works is all assumed to be an ideal constant DC voltage source, whose conclusions may not be fully suitable to the BIC in a hybrid AC/DC microgrid due to the vulnerable DC sub-grid with finite capacity. Making up for this shortcoming, it is revealed in [9], [10] that an asymmetric fault in AC sub-grid will deteriorate DC bus voltage through the coupling of BIC under power control mode. Additionally, DC DERs with different controllers will exhibit different degrees of harmonic interference. Neverthe-

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less, this research, accompanied with the above work, all focus on the pre-fault inverter state of converters with a specific control mode. Whereas BIC can work in both rectifier and inverter states. The bidirectional operating state, as well as the variety of control modes will play significant differences on the fault characteristics, but still haven't been revealed. Therefore, existing study could only provide limited theoretical guidance for the FRT technology and protection design of BIC.

When it comes to FRT control strategies for converters, existing literature can be mainly divided into methods based on improving controllers and the others based on improving the limiter design. In [11], a flexible FRT control strategy based on adapting the outer control loop is presented for current-controlled inverters (such as PQ). It can achieve a dynamic trade-off between active/reactive power oscillation and inrush current suppressions. Similar to these, in [12], a multi-objective FRT control strategy is presented for BIC with power control mode to effectively maintain DC bus voltage without using a chopper circuit. In [13], a FRT control strategy based on switching to the current control mode at the fault time is proposed for voltage-controlled inverters. However, properties such as voltage/frequency support abilities will be lost during the transient process, and another inrush current may occur during the re-switch process. Furtherly, Ref. [14] provide novel FRT methods for droop-controlled inverters in $\alpha\beta$ frame but lacking a certain commonality to other controllers. To address this, many scholars directly analyze and re-design the current and voltage limiters of inverters. It is disclosed in [15]–[18] that conventional limiters may fail to constrain the inrush current under asymmetric fault. In [18], a current limiting method applying in both current and voltage-controlled inverters is discussed to effectively suppress the symmetric/asymmetric fault current. Unfortunately, the above-mentioned FRT strategies all consider the DC side as a constant DC voltage source, and the fault characteristics under a bidirectional operation state have not been taken into account, which are not fully consistent with conditions in a hybrid AC/DC microgrid.

Generally, to the best knowledge of the authors, there is still no in-depth fault analysis for BIC under different control modes in a hybrid AC/DC microgrid. AC fault impact on BIC and on DC bus voltage in the case of bidirectional power flow is still unclear. Additionally, conventional FRT strategies cannot be fully suitable for BIC due to limitations to specific controller, or neglect of the fault characteristics under bidirectional states.

Therefore, as our first motivation, this study comparatively investigates AC fault influence on BIC and DC bus voltage under three commonly used BIC control modes in a hybrid AC/DC microgrid. Based on this, a general accommodative current limiting strategy is proposed for BIC. The main contributions of our study can be summarized as:

1) The influencing mechanism of the BIC control modes, as well as its limiters on the system fault characteristic are revealed by developing a mathematical model and equivalent network of a hybrid AC/DC microgrid. Moreover, both fault conditions under bidirectional power flow of BIC are also

elaborated to disclose the different influences generated by the pre-fault rectifier and inverter states.

2) A general accommodative current limiting method without limitations to control modes and bidirectional power flows is proposed for BIC to prevent inrush current and impact on DC bus voltage by AC faults. Reference current prediction and limitation are performed in abc frame for BIC thermal limitations, and further adjusted in positive/negative sequence dq frames to limit variation/oscillation of DC voltage. Compared with conventional methods, potential current limit failure and distortions under asymmetric faults can be also avoided.

The remainder of this study is organized as follows: In Section II–IV, concepts of different control modes of BIC, and their influence on the fault characteristics of BIC and DC bus voltage are analyzed. In Section V, a comparative summary is drawn. In Section VI, a general accommodative current limiting scheme is presented, accordingly. Finally, experimental verifications are performed in Section VII, followed by conclusions in Section VIII.

II. FAULT ANALYSIS UNDER DC VOLTAGE CONTROL MODE

A. Principle of DC Voltage Control Mode

As shown in Fig. 1, under this control mode, DC bus voltage is maintained by BIC and DC DERs together [19]. Fundamental scheme is shown in Fig. 2, which consists of the outer DC voltage control loop and inner current control loop. The outer loop tracks DC bus voltage and provides references i_{dq}^* for the inner loop as depicted in (1). Afterwards, the inner loop tracks the references to generate the PWM signals [20].

$$i_d^* = (k_{p1} + k_{i1}/s)(V_{dcn} - V_{dc}) \quad (1)$$

where V_{dcn} , V_{dc} , k_{p1} , and k_{i1} represent the rated, actual DC voltage, the proportional and integral parameters, respectively. i_d^* is preferably set to zero since BIC is to control dc bus voltage without providing reactive power to AC sub-grid [21].

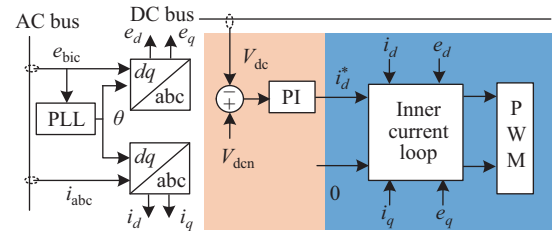


Fig. 2. Principle of DC bus voltage control mode of BIC.

Additionally, as shown in Fig. 2 and (2), BIC will also be configured with current and inner voltage modulation limiters for thermal limitation of power electronic devices.

$$i_{qlim} = \sqrt{i_{lim}^2 - i_{dlim}^2}, \quad e_{qlim} = \sqrt{e_{lim}^2 - e_{dlim}^2} \quad (2)$$

where i_{lim} , e_{lim} , i_{dqlim} and e_{dqlim} refer to the defined current, voltage limitations, and their components in dq frame.

B. Fault Analysis under DC Voltage Control Mode

1) Fault Influence on BIC

The transfer function of BIC including the inner current loop, BIC bridge and filter can be derived as (3). Then, the AC side output current of BIC can be given by (4).

$$G_{\text{bic}}(s) = \frac{(k_{p2}s + k_{i2})(k_{p1}s + k_{i1})}{Ls^3 + (R + k_{p2})s^2 + k_{i2}s} \quad (3)$$

$$i_d = (V_{\text{dcn}} - V_{\text{dc}})G_{\text{bic}}(s) \quad (4)$$

where k_{p2} , and k_{i2} are the proportional and integral parameters in the inner current loop, respectively.

When a symmetric/asymmetric AC fault occurs, V_{dc} in (4) becomes V'_{dc} . Assuming the tracking process is quick, $G_{\text{bic}}(s)$ can be viewed as a “ K ” proportion unit, the post-fault BIC current is

$$i'_d \approx K(V_{\text{dcn}} - V'_{\text{dc}}) \quad (5)$$

where the superscript “ $'$ ” represents the post-fault variables in this paper. Since DC voltage cannot be changed abruptly at the fault time, there will be $V_{\text{dc}} \approx V'_{\text{dc}}$. Thereby, the pre-fault and post-fault current of BIC have similar magnitude under this control mode, that is $i'_d \approx i_d$.

Active power of BIC P'_{bic} after faults occur can be (6). Accordingly, P'_{bic} will be mainly determined by the post-fault AC PCC voltage u'_{ac} since $i'_d \approx i_d$. Its direction is not easy to change accordingly.

$$\begin{cases} P'_{\text{bic}} = 1.5(u'_d i'_{\text{sd}} + u'_q i'_{\text{sq}}) = 1.5u'_d(V_{\text{dcn}} - V'_{\text{dc}}) \\ u'_d = U'^+_{\text{ac}} \sin \varphi'^+ - U'^-_{\text{ac}} \sin(2\omega t - \varphi'^-_{\text{u}}) \\ u'_q = U'^+_{\text{ac}} \cos \varphi'^+ - U'^-_{\text{ac}} \cos(2\omega t - \varphi'^-_{\text{u}}) \end{cases} \quad (6)$$

where U'_{ac} is the amplitude of u'_{ac} , “+”, “−” denote the positive and negative sequence components, φ'_{u} is the initial phase of u'_{ac} .

To reveal the influence of BIC control and the pre-fault power direction on the fault characteristics, Fig. 4 shows the current and power of BIC when u_{ac} asymmetrically drops to 70% u_{n} in cases of pre-fault rectifier and inverter states. As can be observed, the current has small variation under either pre-fault state. While the active/reactive power of BIC possess very small oscillations without direction altered.

2) Fault Influence on DC Bus Voltage

As shown in Fig. 1, the DC sub-grid is equivalent into a DC DER with $V_{\text{dc}} - R$ droop feature [2]. According to the law of conservation of energy, the AC/DC sides active power of BIC should be equal as shown in (7). Hence, the DC bus voltage can be inferred as (8):

$$P'_{\text{bic}} = P'_{\text{bic0}} + A'_{\text{PH}} \sin(2\omega t + \varphi'_{\text{P}}) \quad (7)$$

$$V'_{\text{dc}} = V'_{\text{dc0}} + A'_{\text{VH}} \sin(2\omega t + \varphi'_{\text{V}}) \quad (8)$$

where subscripts “0” and “ A'_{H} ” denote the DC component and amplitude of double frequency oscillation component P'_{bicH} of each variable. φ'_{P} and φ'_{V} are their initial phases, respectively.

According to Fig. 1 and the Kirchhoff’s law of voltage and current, the relationship between P'_{bic0} and V'_{dc0} can be derived

$$V'_{\text{dc0}} = F(P'_{\text{bic0}}) = \frac{-K_2 + \sqrt{K_2^2 + 4K_1 P'_{\text{bic0}}}}{2K_1}$$

$$\begin{aligned} K_1 &= \frac{-(R_1 + R_2)}{R_1 R_{\text{L3}} + R_1 R_2 + R_2 R_{\text{L3}}} \\ K_2 &= \frac{R_2 V_{\text{dcn}}}{R_1 R_{\text{L3}} + R_1 R_2 + R_2 R_{\text{L3}}} \end{aligned} \quad (9)$$

where R_1 , R_2 , and R_{L3} are the equivalent resistances of DC DERs, DC loads, and DC line (from BIC to DC PCC), respectively.

It can be deduced from (9) that V'_{dc0} is related to the equivalent resistances of DC DERs, DC load, DC line, and the interactive active power P'_{bic0} transmitted by BIC. Since the influencing factors of DC sub-grid are immutable, the larger P'_{bic0} will lead to a larger variation of DC bus voltage.

On the other hand, the power oscillation component P'_{bicH} of BIC will cause oscillation of DC current I'_{dcbic} . According to the DC capacitor character, the oscillation component of DC voltage V'_{dcH} can be deduced as

$$\begin{aligned} V'_{\text{dcH}} &= \frac{1}{C_{\text{dc}}} \int I'_{\text{dcbic}} dt = \frac{-A'_{\text{PH}}}{2\omega V'_{\text{dc}} C_{\text{dc}}} \cos(2\omega t + \varphi'_{\text{P}}) \\ &= F(P'_{\text{bicH}}) \end{aligned} \quad (10)$$

As shown in (10), the larger P'_{bicH} and smaller DC capacitor C_{dc} will lead to more intense oscillation of DC voltage. Hence, under this control mode, the variation and oscillation of DC voltage is mainly determined by the fault voltage u'_{ac} since there is $i'_d \approx i_d$. As shown in Fig. 3, the post-fault DC voltage remains stable with very little oscillation regardless BIC operates in the pre-fault rectifier or inverter state.

Generally, the equivalent networks of hybrid AC/DC microgrid under AC fault when BIC operates in DC voltage control mode is shown in Fig. 4. In the studied system, BIC is ungrounded while the AC sub-grid can be viewed as a grounded system. Hence, the zero-sequence network is neglected due to the lack of passageway for zero sequence current. In the AC sub-grid, BIC is equivalent to a controlled current source in parallel with a capacitor. While in the DC sub-grid, BIC is equivalent to a controlled DC voltage source in series with a controlled double frequency voltage source. Moreover, no matter BIC operates as a rectifier or inverter initially, AC faults can hardly lead to a serious overcurrent of BIC or severe influence on DC sub-grid.

III. FAULT ANALYSIS UNDER POWER CONTROL MODE

A. Principle of Power Control Mode

The power control mode of BIC flexibly promotes mutual power support between sub-grids by bus signals. As indicated in Fig. 5, the controller consists of outer power loop and inner current loop [2], [5]. Principle of the outer loop is shown in (11)–(12), the error between the normalized deviations of AC bus frequency and DC bus voltage will pass through a PI unit to generate the inner current reference i^*_{dq} .

$$i^*_d = 2P^*/3U_{\text{ac}} = 2G_{\text{PI}}(t)(V_{\text{pu}} - f_{\text{pu}})/3U_{\text{ac}} \quad (11)$$

$$\begin{aligned} f_{\text{pu}} &= [f - 0.5(f_{\text{max}} + f_{\text{min}})]/0.5(f_{\text{max}} - f_{\text{min}}) \\ &= (f - f_{\text{n}})k_{\text{f}} \end{aligned}$$

$$\begin{aligned} V_{\text{pu}} &= [V_{\text{dc}} - 0.5(V_{\text{max}} + V_{\text{min}})]/0.5(V_{\text{max}} - V_{\text{min}}) \\ &= (V - V_{\text{dcn}})k_{\text{V}} \end{aligned} \quad (12)$$

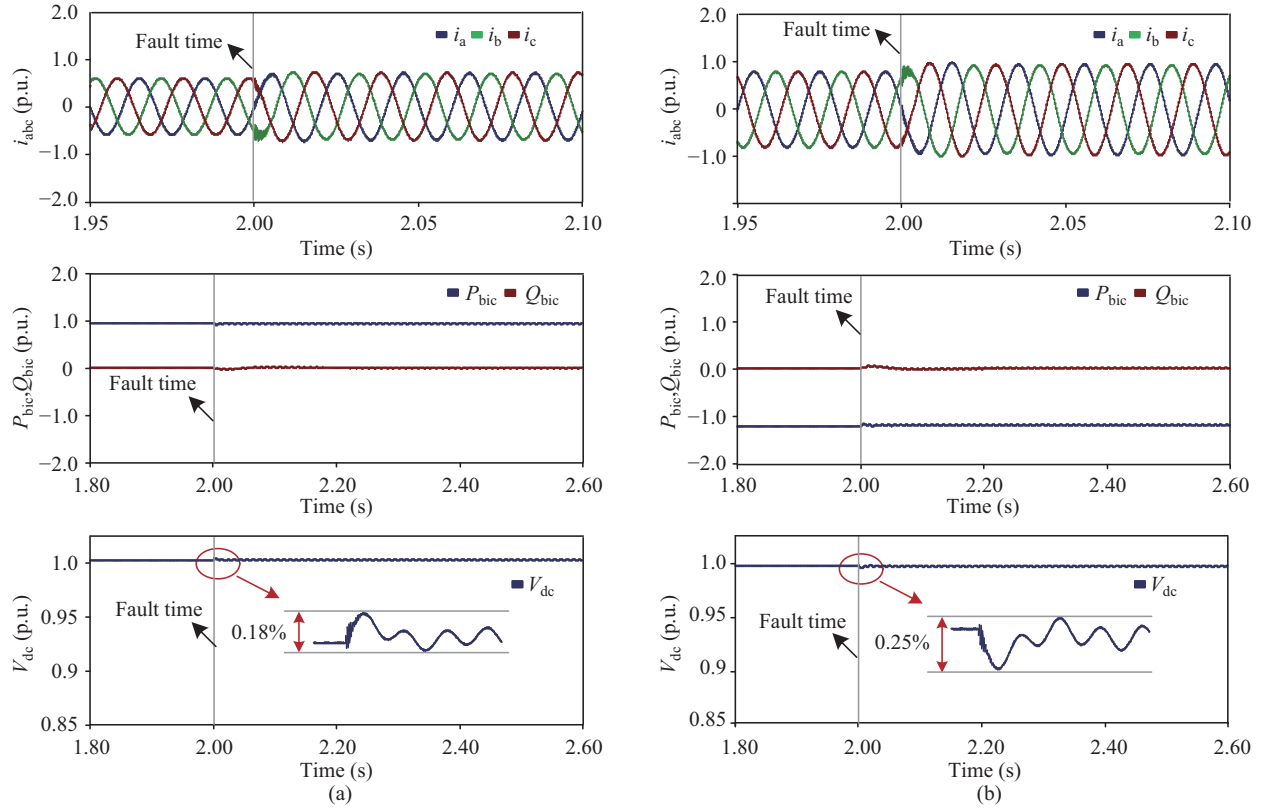


Fig. 3. Current, active/reactive power of BIC, and DC bus voltage when BC phase of u_{ac} asymmetrically drop to 70% u_n under DC voltage control mode. (a) Results when BIC operates as an inverter at the pre-fault. (b) Results when BIC operate as rectifier at the pre-fault.

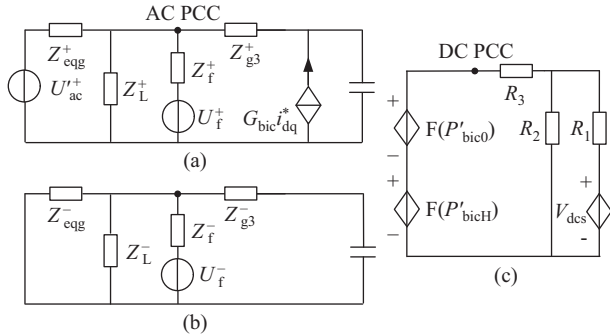


Fig. 4. Equivalent networks of hybrid AC/DC microgrid when BIC operates in DC voltage control mode. (a) Positive sequence networks of AC sub-grid. (b) Negative sequence networks of AC sub-grid. (c) Network of DC sub-grid.

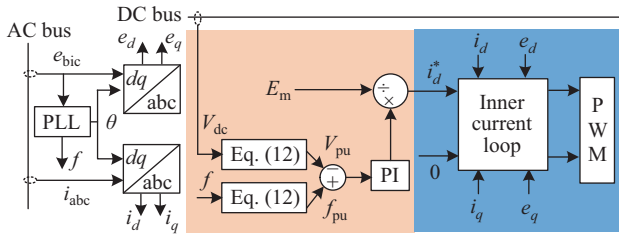


Fig. 5. Principle of power control mode of BIC.

where f_n , f_{max} , V_{max} , f_{min} , and V_{min} are the rated, maximum, and minimum values of AC bus frequency and DC bus voltage, respectively. V_{pu} and f_{pu} are their normalized values. P^* represents the calculated reference active power of BIC.

B. Fault Analysis under Power Control Mode

1) Fault Influence on BIC

Under this control mode, the transfer function including the inner loop, BIC bridge and filter is similar to (3). Hence, when a symmetric/asymmetric AC fault occurs, BIC current can be:

$$i_d' = \frac{\left(\frac{2K[k_f(f_0' + A'_{fH} \sin(2\omega t + \varphi_f') - f_n) - k_V(V'_{dc} - V_{dcn})]}{3(U'_{ac0} + A'_{UH} \sin(2\omega t + \varphi_U'))} \right)}{3(U'_{ac0} + A'_{UH} \sin(2\omega t + \varphi_U'))} \quad (13)$$

where subscript "0" represents the DC components, A'_{fH} , A'_{UH} , φ_f' , and φ_U' are the amplitude of oscillation components, and their initial phases. Coefficients k_V and k_f determine fault current sensitivity to variations of bus signals. In the event of symmetric fault, oscillation components are ignored. As shown in (13), post-fault BIC current is determined by the frequency, amplitude of AC bus voltage and V'_{dc} at the fault time. Moreover, it will contain harmonic components due to oscillations of AC frequency.

Under the power control mode, P'_{bic} can be derived as (14). Post-fault power direction depends on the error between variations of AC frequency and DC voltage.

$$P'_{bic} = \frac{\left(\frac{3K^2 u_d' [k_f(f_0' + A'_{fH} \sin(2\omega t + \varphi_f') - f_n) - k_V(V'_{dc} - V_{dcn})]}{3(U'_{ac0} + A'_{UH} \sin(2\omega t + \varphi_U'))} \right)}{3(U'_{ac0} + A'_{UH} \sin(2\omega t + \varphi_U'))} \quad (14)$$

To disclose the influence of this control mode and pre-fault power direction of BIC, Fig. 6 shows the fault response when

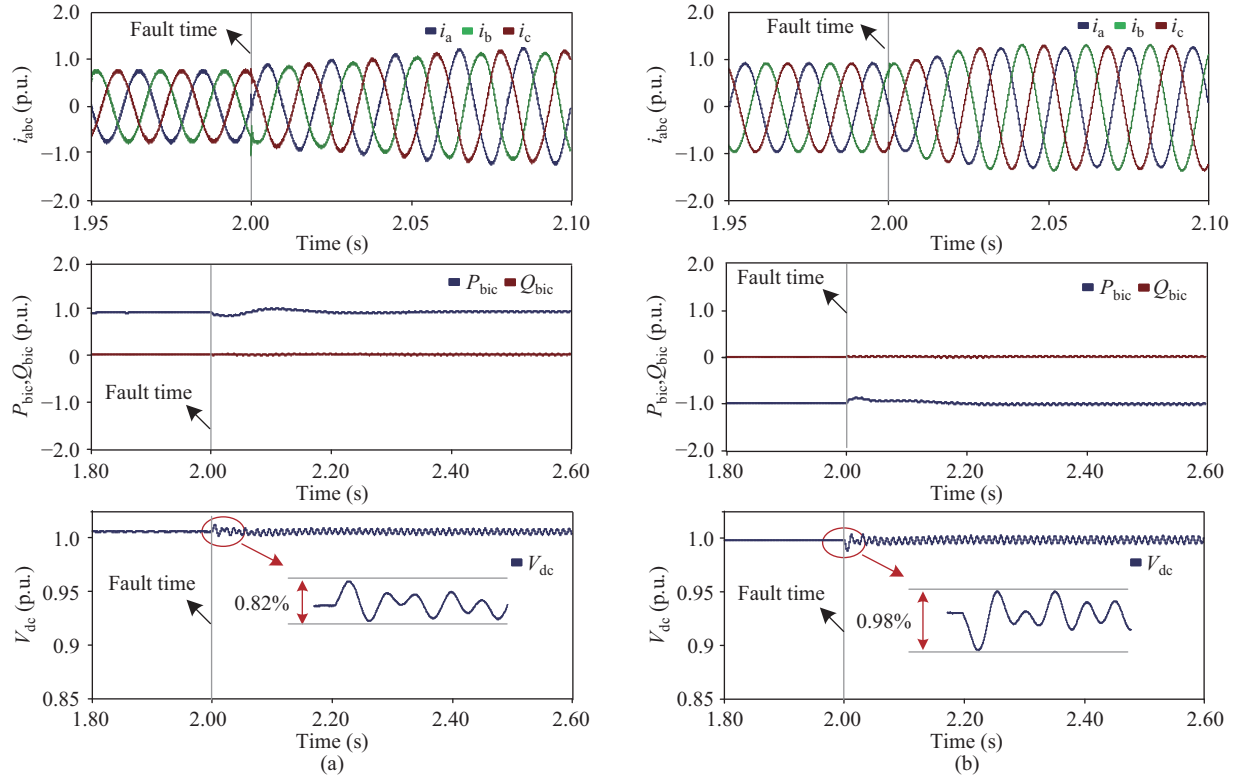


Fig. 6. Current, active/reactive power of BIC, and DC bus voltage when BC phase of u_{ac} asymmetrically drop to 70% u_n under power control mode. (a) Results when BIC operate as an inverter at the pre-fault. (b) Results when BIC operate as a rectifier at the pre-fault.

u_{ac} asymmetrically drops to 70% u_n in cases of both pre-fault rectifier and inverter states. As illustrated in Fig. 6, BIC current is similar to an asymmetric step response with small oscillations in either the pre-fault state is rectifier or inverter. The active/reactive power of BIC has a small overshoot at the fault time without power direction conversion.

2) Fault Influence on DC Bus Voltage

Referring to (9-10), and (14), under the power control mode, V'_{dc} will be less affected since P'_{bic} is similar to its pre-fault value. As shown in Fig. 6, when u_{ac} asymmetrically drop to 70% u_n , DC voltage only contains small oscillations.

Generally, under this control mode, BIC can be equivalent to a controlled current source when AC faults occur. The equivalent networks of hybrid microgrids during fault are similar to that in Fig. 4. Since double frequency oscillations in the AC voltage and frequency will be introduced into the controller during asymmetric fault, the current and power directions of BIC, as well as the DC bus voltage are more heavily impacted compared to that under DC voltage control mode.

IV. FAULT ANALYSIS UNDER AC VOLTAGE CONTROL MODE

A. Principle of AC Voltage Control Mode

Principle of the AC voltage control mode of BIC is shown in Fig. 7, including an outer AC voltage control loop and an inner current loop. The outer loop aims to maintain AC bus voltage, as shown in (15) and provides references i_{dq}^* for the inner loop [4], [5].

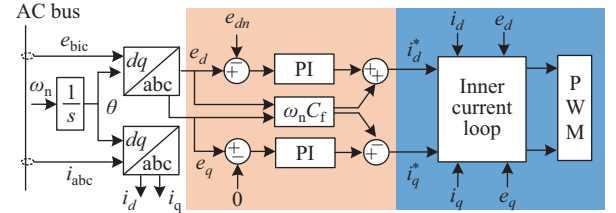


Fig. 7. Principle of AC voltage control mode of BIC.

$$i_{dq}^* = G_{PI}(t)(e_{dq} \pm e_{dq}) \pm j\omega_n C_f \quad (15)$$

where e_{dq} , e_{dq} are the dq components of rated and detected AC side terminal voltage of BIC. C_f is the filter capacitor of BIC.

B. Fault Analysis under AC Voltage Control Mode

1) Fault Influence on BIC

According to Fig. 7, transfer function of BIC under this control mode is given by (16). τ_i represents time constant of the inner current control loop. k_{vp} , k_{vi} denote parameters of PI unit. AC side terminal voltage of BIC e_{bic} is still controllable under this control mode. As shown in Fig. 1, BIC current amplitude I'_m is determined by the error between the AC bus voltage u'_{ac} and e'_{bic} , which can be expressed as (17).

$$e_{dq} = G_e(s)e_{dq} - Z(s)i_{dq} \quad (16)$$

$$G_e(s) = \frac{k_{vp}s + k_{vi}}{\tau_i C_f s^3 + C_f s^2 + k_{vp}s + k_{vi}}$$

$$Z(s) = \frac{\tau_i s^2}{\tau_i C_f s^3 + C_f s^2 + k_{vp} s + k_{vi}}$$

$$I'_m = \frac{|e'_{bic} - u'_{ac}|}{\sqrt{R^2 + (\omega L)^2}} \quad (17)$$

where $Z_{g3} = R + j\omega L$, which includes the filter impedance of BIC and line impedance between AC PCC and BIC.

As shown in (17), when the AC fault occurs, u_{ac} will drop immediately, while the midpoint voltage of BIC cannot be changed abruptly and still remains symmetrical at the fault time. Therefore, a small difference between u'_{ac} and e'_{bic} will directly cause rapid inrush current of BIC since Z_{g3} is small. In this event, limiters can be easily activated with two cases accordingly.

Case I: when only current limiter is activated, BIC is equivalent to a constant current source, $I'_m = I_{lim}$. Then there is:

$$\begin{cases} P'_{bic} = 1.5(u'_d i_{dlim} + u'_q i_{qlim}) \\ Q'_{bic} = 1.5(u'_d i_{qlim} - u'_q i_{dlim}) \end{cases} \quad (18)$$

Case II: When a voltage limiter is activated, this denotes effectiveness of the current limiter has been destroyed. This could occur especially when an asymmetric fault occurs (Although the amplitude of current is limited by the current limiter in dq frame, the actual current in abc frame may not be accurately limited [15]–[17]) or when Z_{g3} is large. Upon this, voltage of the overcurrent phase may larger than limitations, i.e., $e'_{bic} = i'_{abc} \cdot Z_{g3} \geq e_{lim}$. BIC will turn into a constant voltage source. Then the BIC current amplitude will be (19), and P'_{bic} can be (20). As can be observed from (18) and (20),

power direction is prone to convert into inverter state positive (i.e., $P'_{bic} > 0$) since there is often $e_{dqlim} > u'_{dq}$.

$$I'_m = \frac{|e_{lim} - u'_{ac}|}{\sqrt{R^2 + (\omega L)^2}} \quad (19)$$

$$\begin{cases} P'_{bic} = 1.5(u'_d(e_{dlim} - u'_d)/Z_d + u'_q(e_{qlim} - u'_q)/Z_q) \\ Q'_{bic} = 1.5(u'_d(e_{qlim} - u'_q)/Z_q - u'_q(e_{dlim} - u'_d)/Z_d) \end{cases} \quad (20)$$

To identify the influence of the control and pre-fault power direction of BIC, Fig. 8 shows the fault response when u_{ac} asymmetrically drop to 70% u_n . As can be seen, BIC suffers from large inrush current with severe distortions (about $3I_n$ within 10 ms), which denotes the current limiter has been destroyed. The active and reactive power of BIC increase with intense oscillations. Moreover, regardless of the pre-fault power direction, it is prone for BIC to shift into the inverter state after the fault occurs.

2) Fault Influence on DC Bus Voltage

The fault influence on DC voltage under this control mode can be deduced by combining (9)(18)(20). If only current limiter is activated as in case I, the larger u_{ac} will lead to the larger P'_{bic} , and consequently, a larger DC voltage deviation. In case II, if voltage limiter is activated, the variation/oscillation of V_{dc} depends on e_{lim} , Z_3 , and u'_{ac} at the fault time since P'_{bic} is directly determined by these as in (20). As shown in Fig. 8, the DC voltage suffers from serious sag (around 10% V_{dcn}) and oscillations under the same fault condition. Additionally, the impact on V_{dc} are both severe either the pre-fault state is rectifier or inverter. Note that the deteriorated V_{dc} also worsen the distortion of the AC side current of BIC.

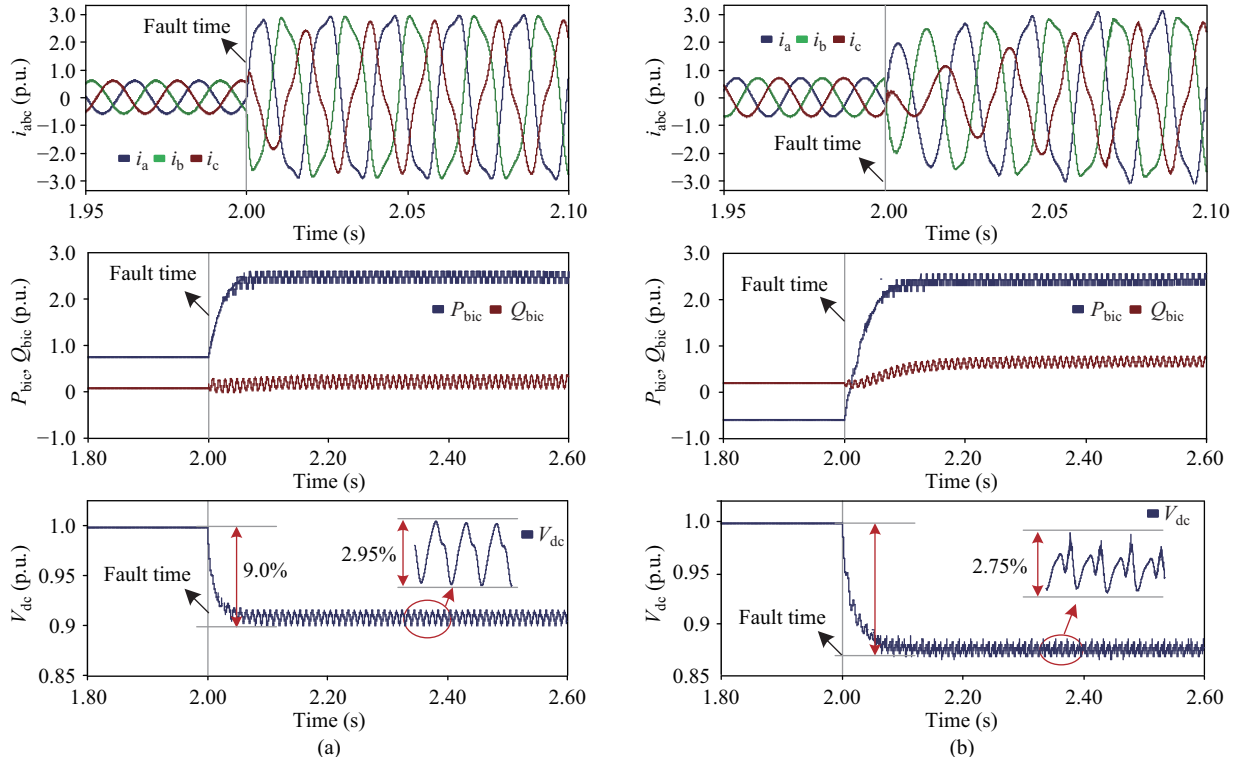


Fig. 8. Current, active/reactive power of BIC, and DC bus voltage when BC phase of u_{ac} asymmetrically drop to 70% u_n under AC voltage control mode. (a) Results when BIC operate as an inverter at the pre-fault. (b) Results when BIC operate as a rectifier at the pre-fault.

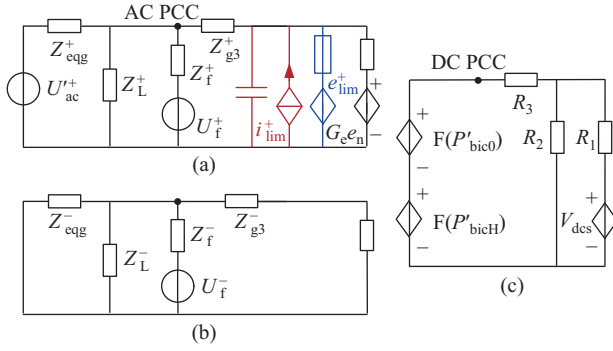


Fig. 9. Equivalent networks of hybrid AC/DC microgrid when BIC operates in AC voltage control mode. (a) Positive sequence network of AC sub-grid. (b) Negative sequence network of AC sub-grid. (c) Network of DC sub-grid.

Generally, under this control mode, the equivalent networks of hybrid AC/DC microgrid is illustrated in Fig. 9. In the AC sub-grid, BIC is equivalent to a constant current source in parallel with capacitor when only the current limiter is activated (red), and a constant voltage source in series with output impedance when voltage limiter is activated (blue), respectively. BIC is still equivalent to two series-controlled DC voltage source in the DC sub-grid. However, BIC easily suffers from overcurrent with distortions especially when asymmetric faults occur even with limiters, the power direction is easily converted into inverter state, and the DC bus voltage undergoes large variations and oscillations.

V. COMPARISON AND SUMMARY

Based on the above analysis, comparisons among different control modes under the same pre-fault state, as well as comparisons between results under pre-fault rectifier and inverter state of a specific control mode are summarized in this section. Relevant data results are shown in Table I for a more distinct comparison. Note the conditions for the calculated data in Table I stay similar except for the BIC control system. The physical circuit and control parameters are shown in Table II in Section V. The fault event is set as a two-phase grounded fault (*BC phases* of u_{ac} asymmetrically dip to 70% u_n) since it is relatively more severe than the other asymmetric faults. Moreover, under either pre-fault rectifier or inverter states, the BIC operates around the rated power state initially.

TABLE I
COMPARATIVE SUMMARIZES

Control mode	Peak of i_{abc} (p.u.)		Deviation of V_{dc} (ΔV_{dc} %)		Distortion of i_{abc} (THD %)	
	Inv.	Rec.	Inv.	Rec.	Inv.	Rec.
DC voltage control	1.20	1.19	0.18	0.25	1.12	1.13
Power control	1.41	1.38	0.82	0.98	2.52	1.71
AC voltage control	3.63	3.72	9.0	14.0	13.75	13.38

1) *Comparison of BIC's peak current*: To avoid the damage of BIC due to the limited thermal capacity, it is significant to figure out the peak current upon AC fault. As shown in Table I, under the same pre-fault state, BIC with AC voltage control mode suffer from the most serious inrush current, followed by that under the power control mode, and DC voltage control

mode. While for a specific mode, the current responses are similar either in the pre-fault rectifier or inverter state.

2) *Comparison of power direction*: It is more likely for BIC to convert into the inverter state at fault time under AC voltage control mode than under DC voltage and power control modes.

3) *Comparison of DC bus voltage variation/oscillation*: DC bus voltage undergoes the most severe deviations under AC voltage control mode, and least under DC voltage control mode. Meanwhile, for a specific mode, deviations in the case of a pre-fault rectifier state tends to be larger than in the case of a pre-fault inverter state. Additionally, it is revealed that if only the current limiter is activated, the smaller dip of u_{ac} will lead to a larger deviation. While if the voltage limiter is activated, situations are the opposite.

4) *Comparison of BIC current distortion*: distortion of BIC current is caused by negative sequence components in the event of an asymmetric fault, the limiter, and the reversely coupling effect of deteriorated DC voltage. Consequently, based on the former results, under AC voltage control mode, distortion of BIC current ranks the highest either in the pre-fault rectifier or inverter state.

Generally, it can be concluded that situations under AC voltage control mode tends to be the most severe, followed by that under the power and DC voltage modes. Therefore, effective current limiting strategy with considerations of fault characteristics is necessary for BIC to ensure safe and reliable operation of a hybrid AC/DC microgrid.

VI. ACCOMMODATIVE CURRENT LIMITING METHOD FOR BIC

As can be inferred from the former analysis the outer loop of different control modes is the key to differences in the fault characteristics. Therefore, we proposed a general accommodative current limiting strategy by accommodating the current references generated by the outer loop. It can be extended to all three commonly used control modes with bidirectional operation states to effectively suppress BIC fault inrush current, and meanwhile reduce variation/oscillation of DC bus voltage in the event of symmetric/asymmetric faults. Additionally, power quality of BIC current and DC sub-grid can be improved, which benefits both AC and DC loads. Since situations under AC voltage control modes rank the most severe, here we take this mode as an application example, the overall control scheme is shown in Fig. 10.

At first, a positive and negative sequence separation is performed. Afterwards, the current references for inner loop is predicted rapidly and limited in *abc* frame, so that the inrush current of BIC will be constrained for the thermal limitations of power electronic devices. Subsequently, for the sake of relieving the impact of AC faults on DC bus voltage, the maximum positive and negative sequence reference current in *dq* frame is predicted using real-time AC voltage. Current is further constrained according to the relationship between the maximum allowable variation/oscillation of DC bus voltage and the active power of BIC. Specific principles will be discussed as follows.

$$i_{dqref3}^k = \begin{cases} \frac{i_{dq\max}^k}{i_{dqref2}^k} i_{dqref2}^k, & i_{dqref2}^k \geq i_{dq\max}^k \\ i_{dqref2}^k, & i_{dqref2}^k < i_{dq\max}^k \end{cases} \quad (28)$$

where i_{dqref3}^k and i_{dqref2}^k are the limited and original current references in dq frame, respectively.

Subsequently, as shown in the right block in Fig. 11, after the current limiting in abc frame, the three-phase current will be transformed into the positive and negative sequence networks by SOGI and be further constrained by (28) to help limit the variation/oscillation of DC voltage by concrete requirements. Upon this, reliability and quality of the power supply of DC microgrid can be guaranteed, which could also reduce the coupling influence on the voltage and current of AC sub-grid.

VII. EXPERIMENTAL STUDY

In order to demonstrate effectiveness of the proposed method, hardware-in-the-loop experiments with topology in Fig. 1 are carried out, including performance verifications under the symmetric/asymmetric faults, as well as pre-fault inverter and rectifier states. Since the fault conditions under AC voltage control mode rank the most serious, here we also take it as an example [23]. Further, for a more intuitive understanding, each group of experiments is compared with conventional method with fixed limiters. The experimental platform is shown in Fig. 12, wherein, the physical circuit of a hybrid AC/DC microgrid is performed by the real-time on the simulator OP5607 equipped with FPGA-based inputs and outputs (I/Os) board. The control system consists of three digital signal processors (DSP TMS320F28335) for AC/DC sub-grids and BIC, respectively. Relevant circuit and control parameters are shown in Table II. Fault time is set as $t = 0.3$ s. Additionally, to fully verify the function of DC bus voltage deviation/ oscillation reduction with proposed method,

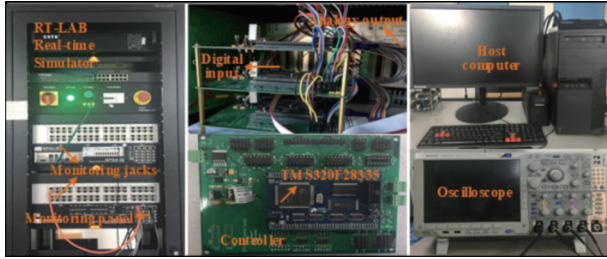


Fig. 12. Experimental platform.

TABLE II
PHYSICAL CIRCUIT AND CONTROL PARAMETERS

Parameter	Value	Parameter	Value
P_{bicn} (kW)	15	L_{acf} (mH)	3
Q_{bicn} (kvar)	0	C_{acf} (μ F)	10
E_n (V)	311	C_{dc} (mF)	2.5
f_n (Hz)	50	R_{L1} (Ω)	0.2
V_{dcn} (V)	800	R_{L2} (Ω)	0.2
$Z_{g2,3}$ (Ω)	$0.2 + 1.2j$	R_{L3} (Ω)	0.2
Z_{g1} (Ω)	$0.1 + 0.4j$	P_{acsn} (kW)	20
P_{dcscn} (kW)	20	Q_{acscn} (kvar)	0
$f_{min} - f_{max}$ (Hz)	49.8–50.2	$V_{min} - V_{max}$ (V)	760–840

the maximum allowable variation of the DC bus voltage are equal to $\pm 5\%$ and $\pm 10\%$ under the pre-fault inverter and rectifier state, respectively, since there will be larger deviations under the later pre-fault condition according to the previous theoretical analysis.

A. Performance When Subjected to Symmetric AC Faults

This group of experiments aims to verify the performance of proposed method under a symmetric fault with both pre-fault inverter and rectifier states of BIC. The experimental results of conventional method and of proposed method when subjected to a symmetric fault under AC voltage control mode with pre-fault inverter state are shown in Figs. 13–14, respectively. As can be observed in Fig. 13(a) and Fig. 14(a), the fault current of the BIC can be well limited within twice the rated value $2I_n$. However, the sag of DC bus voltage V_{dc} as shown in Fig. 13(c) will be larger with conventional method. This is because, although the BIC current has been limited to $2I_n$, the transmission power of the BIC will be large with a small AC PCC voltage dip, therefore, indirectly influencing V_{dc} . These are consistent with the theoretical analysis in Section IV. On the other hand, as shown in Fig. 14(c), with proposed method, the DC bus voltage can be well maintained within its

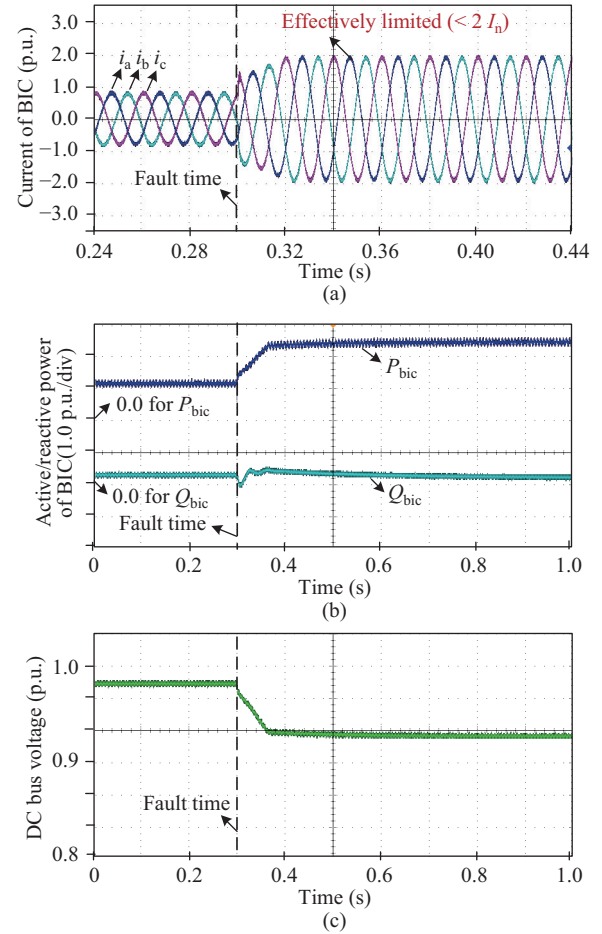


Fig. 13. Experimental results of conventional method when subjected to a symmetric fault (u_{abc} dip to around 87% of the rated value) under AC voltage control mode with pre-fault inverter state. (a) Current of BIC. (b) Active/reactive power of BIC. (c) DC bus voltage.

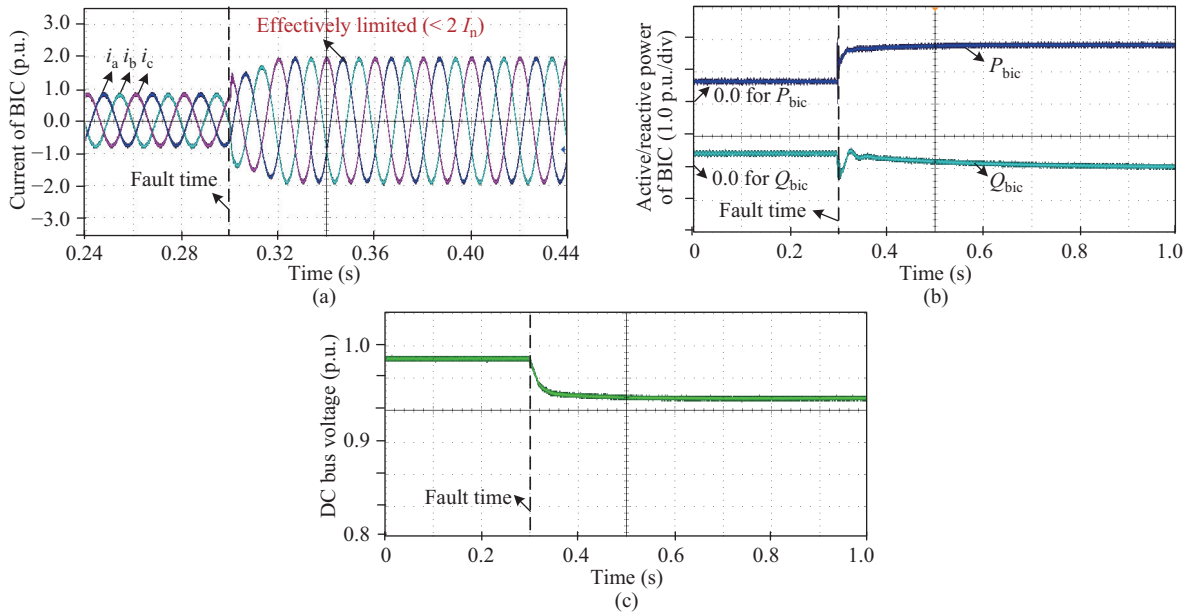


Fig. 14. Experimental results of proposed method when subjected to a symmetric fault (u_{abc} dip to around 87% of the rated value) under AC voltage control mode with pre-fault inverter state. (a) Current of BIC. (b) Active/reactive power of BIC. (c) DC bus voltage.

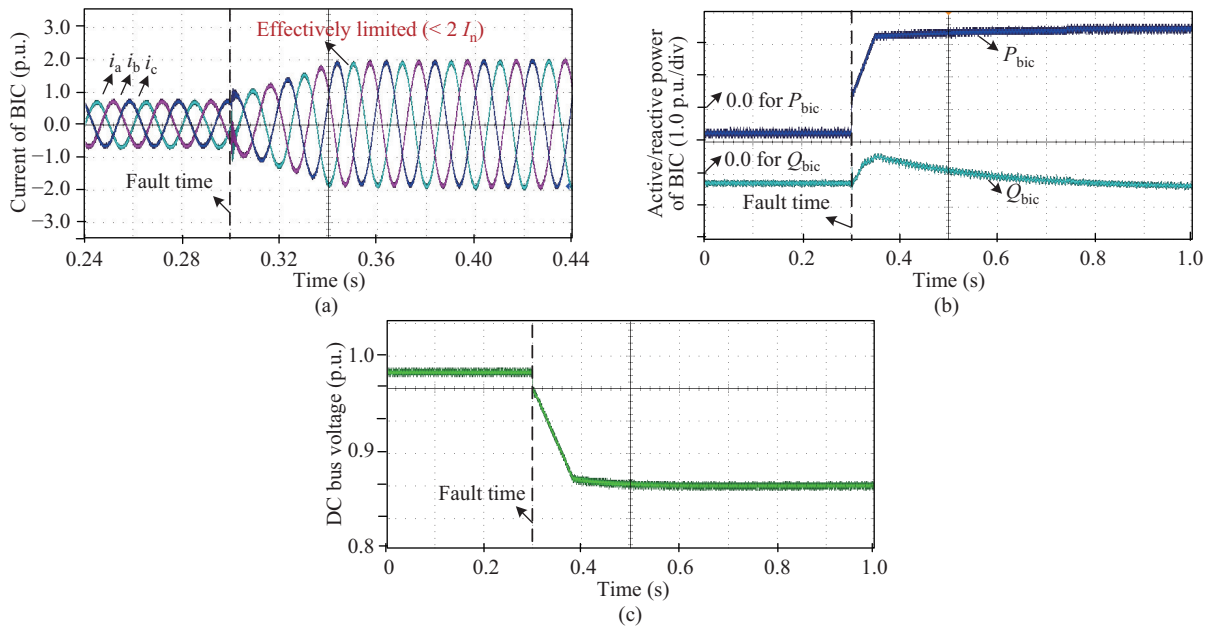


Fig. 15. Experimental results of conventional method when subjected to a symmetric fault (u_{abc} dip to around 87% of the rated value) under AC voltage control mode with pre-fault rectifier state. (a) Current of BIC. (b) Active/reactive power of BIC. (c) DC bus voltage.

allowable range 5% since the actual current reference has been accommodatively limited with consideration of the deviation of V_{dc} , which can also be indicated by the reduced active power Fig. 14(c).

Figures 15–16 show the experimental results of conventional method and of proposed method when subjected to a symmetric fault under AC voltage control mode with pre-fault rectifier state, respectively. Similar phenomena can be viewed as results under pre-fault inverter state. Moreover, it is obvious that the DC bus voltage can be well maintained within the previous set value 10% with proposed method. Accordingly, in this case, the active power of BIC as shown in Fig. 16(c)

is also relatively larger than in Fig. 14(c).

Generally, both the conventional method and the proposed method can achieve good current limitation performance of BIC under symmetric faults. However, only with proposed method, the DC bus voltage can be accurately maintained.

B. Performance When Subjected to Asymmetric AC Faults

This group of experiments aims to verify performance of the proposed method under asymmetric faults with both pre-fault inverter and rectifier states of BIC.

Figure 17 shows the experimental results of conventional method when subjected to a two-phase grounded fault (u_b

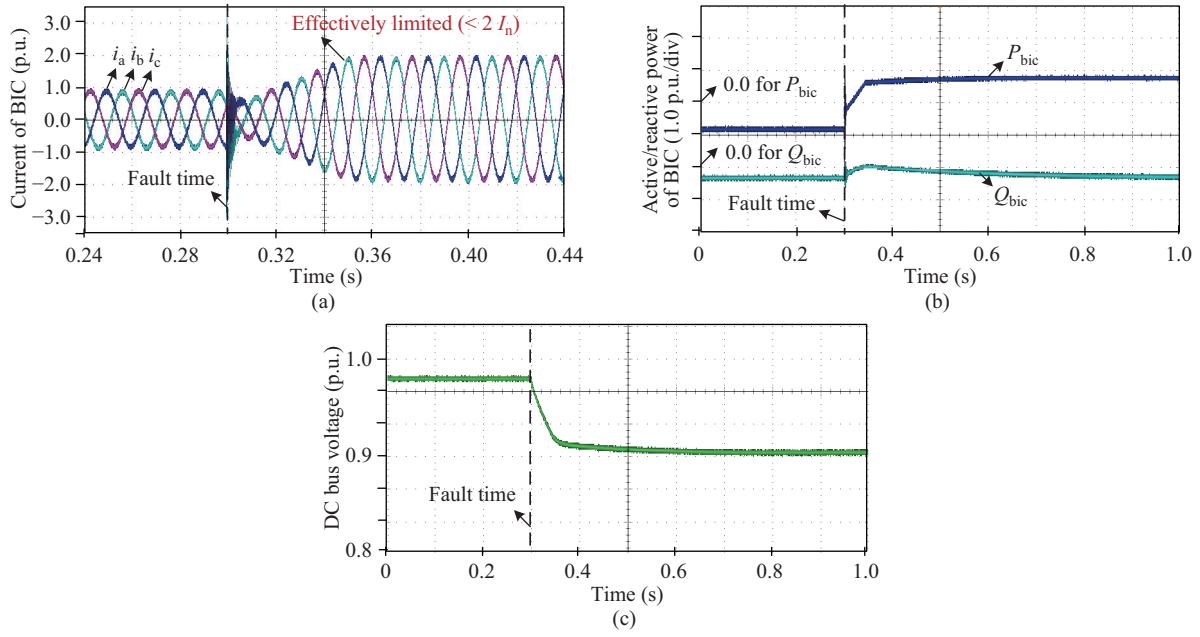


Fig. 16. Experimental results of proposed method when subjected to a symmetric fault (u_{abc} dip to around 87% of the rated value) under AC voltage control mode with pre-fault rectifier state. (a) Current of BIC. (b) Active/reactive power of BIC. (c) DC bus voltage.

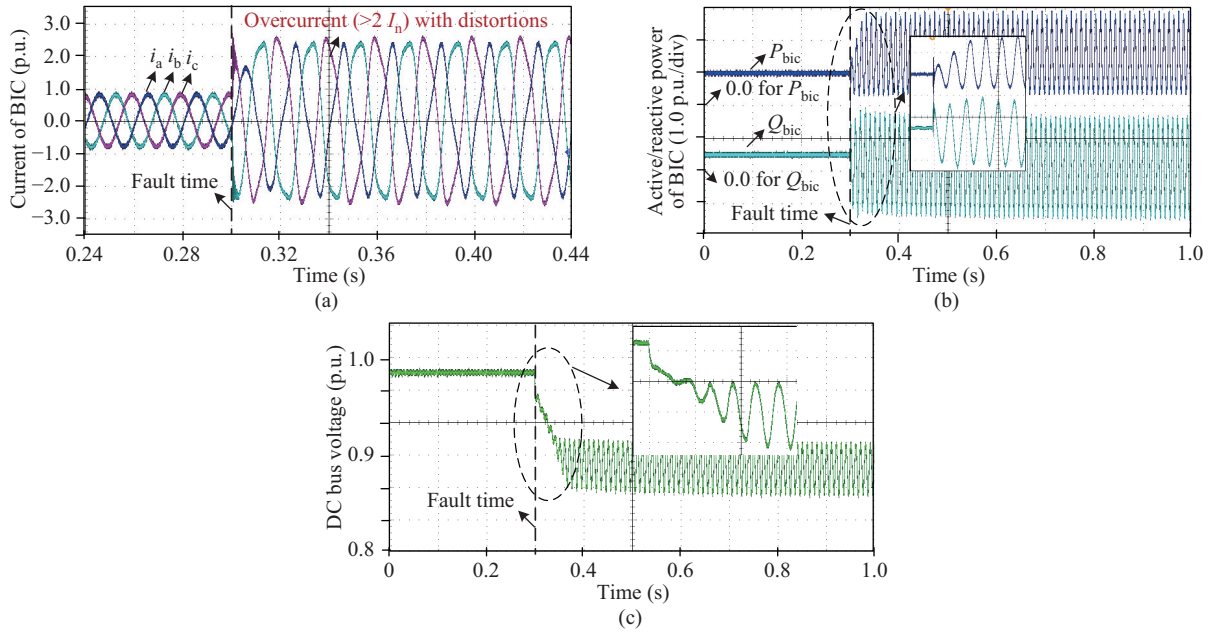


Fig. 17. Experimental results of conventional method when subjected to a two-phase grounded fault (u_b and u_c drop to 70% u_n) under AC voltage control mode with pre-fault inverter state. (a) CURRENT of BIC. (b) Active/reactive power of BIC. (c) DC bus voltage.

and u_c drop to 70% u_n) under AC voltage control mode with pre-fault inverter state. AC side current of BIC has inrush over $2I_n$ within 10 ms with distortions as shown in Fig. 17(a). The BIC suffers from intense power oscillations and active/reactive power interactions all increase. The sag of DC bus voltage has already reached 8.6% V_{dcn} . Moreover, intense oscillations are contained. These results are consistent with the simulation results of Fig. 8 and indicate the safety of BIC and the reliability of DC sub-grid have been threatened.

Figure 18 shows the experimental results of proposed method under the same fault condition with pre-fault inverter

state. The minimum DC bus voltage oscillation restraint are set as 2% V_{dcn} . As shown in Fig. 18(a), the proposed method can effectively maintain BIC current within its maximum allowable upper limit with less distortions. As shown in Fig. 18(b), the oscillation amplitudes of active/reactive power of BIC have been greatly alleviated compared with that in with Fig. 17(b). As shown in Fig. 18(c), the DC bus voltage sag has been restrained within 5% V_{dcn} , and the oscillation amplitude has been reduced from 3.7% V_{dcn} to around 2% V_{dcn} , compared with that in Fig. 17(c). Therefore, experimental results effectively verify feasibility of the proposed method.

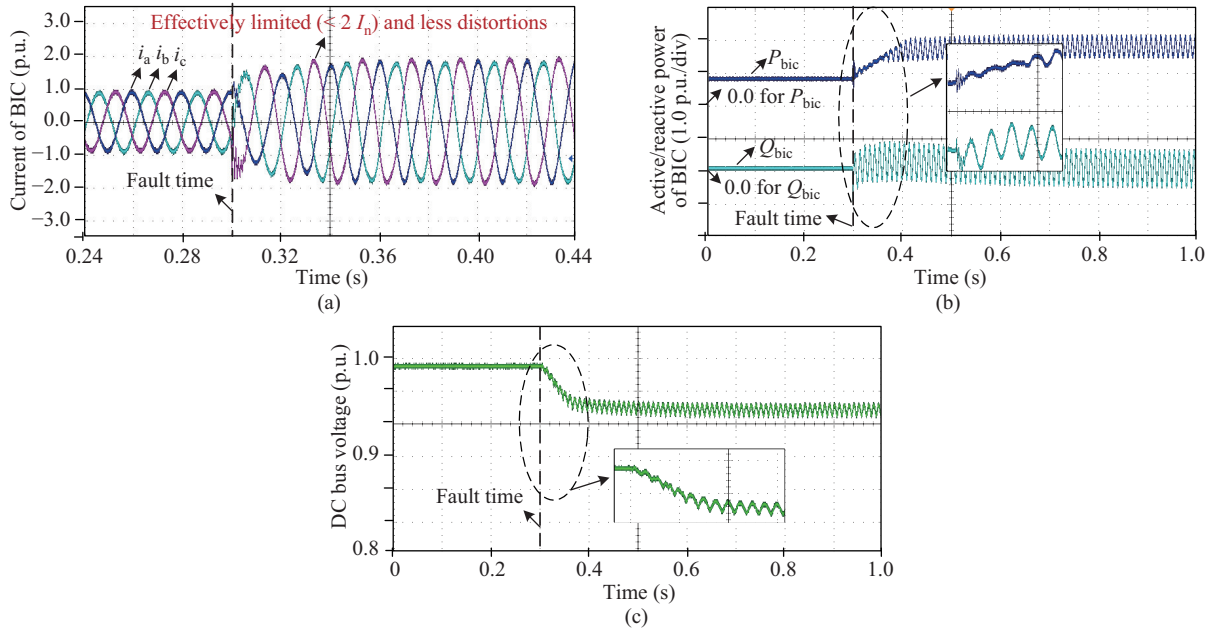


Fig. 18. Experimental results of proposed method when subjected to a two-phase grounded fault (u_b and u_c drop to 70% u_n) under AC voltage control mode with pre-fault inverter state. (a) Current of BIC. (b) Active/reactive power of BIC. (c) DC bus voltage.

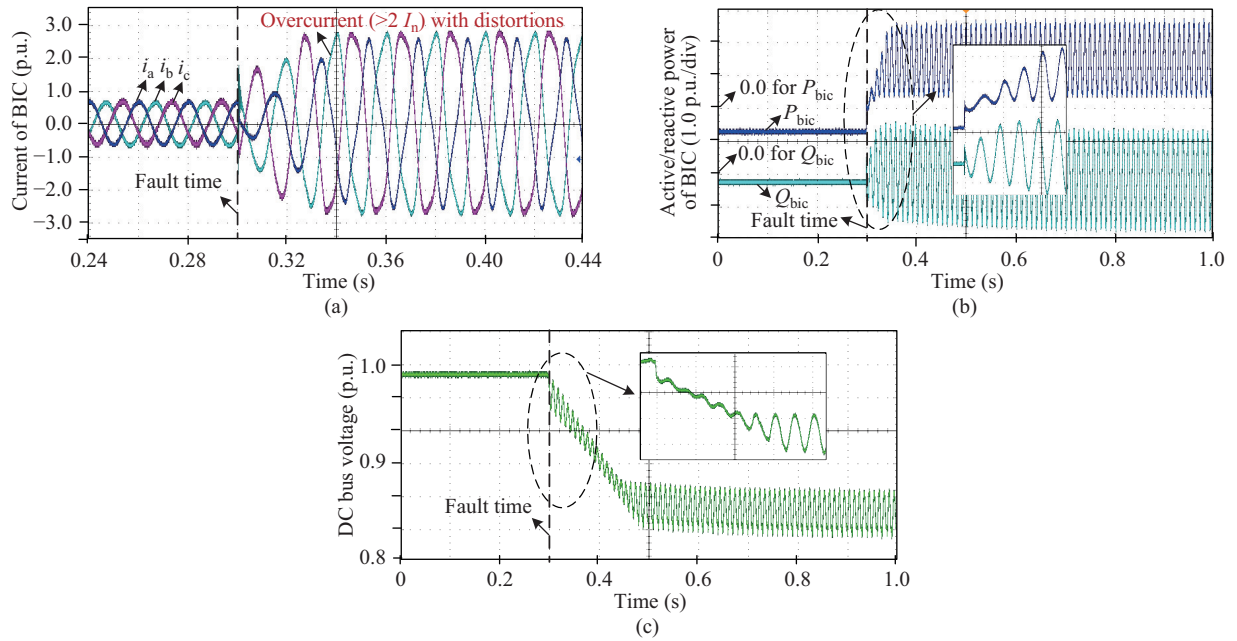


Fig. 19. Experimental results of conventional method when subjected to a two-phase grounded fault (u_b and u_c drop to 70% u_n) under AC voltage control mode with pre-fault rectifier state. (a) Current of BIC. (b) Active/reactive power of BIC. (c) DC bus voltage.

Experimental results of conventional method and of the proposed method when subjected to an asymmetric fault under AC voltage control mode with pre-fault rectifier state are shown in Figs. 19–20. With conventional method, similar inrush current with distortions, and more serious deviation of DC bus voltage (around 12% V_{dcn}) than under pre-fault inverter state can be observed. While with the proposed method, objectives of both the BIC fault current limitation with less distortions and the deviation/oscillation restrain of DC bus voltage (within the set value 10% V_{dcn}) can be achieved under asymmetric faults.

Generally, through the above two groups of experimental

results, effectiveness of the proposed method under the symmetric/asymmetric faults, as well as under pre-fault inverter/rectifier states can be well demonstrated.

VIII. CONCLUSION

This study investigates AC fault influence on BIC and DC bus voltage under three commonly used modes of BIC with bidirectional pre-fault states in a hybrid AC/DC microgrid. Based on this theoretical analysis, an accommodative current limiting method is also presented for BIC. Conclusions are drawn as follows:

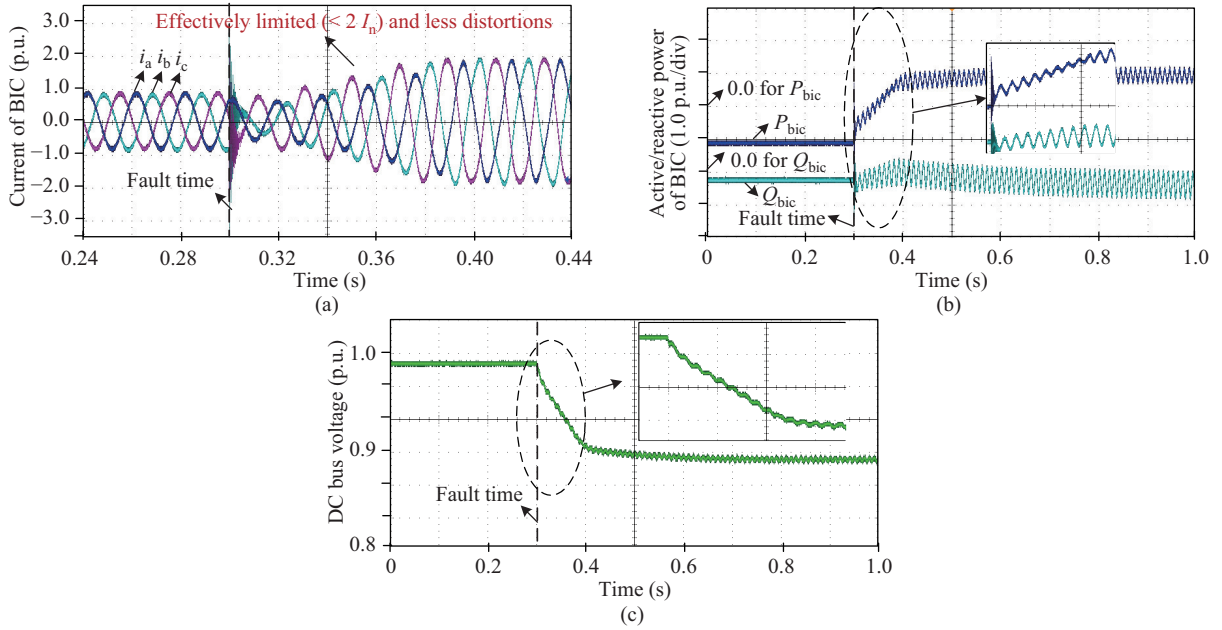


Fig. 20. Experimental results of proposed method when subjected to a two-phase grounded fault (u_b and u_c drop to 70% u_n) under AC voltage control mode with pre-fault rectifier state. (a) Current of BIC. (b) Active/reactive power of BIC. (c) DC bus voltage.

1) BIC control mode dominates AC fault influence on BIC and the DC bus voltage. It is found that under DC voltage control mode, BIC would be hardly driven into an overcurrent state with DC voltage being less affected. Conditions under the power control mode rank second. Nevertheless, under AC voltage control mode, large inrush current with distortions in BIC is observed in a few milliseconds with DC bus voltage suffering from severe variation and oscillations.

2) Fault characteristic comparisons among the three control modes remains unchanged regardless of the pre-fault state. However, for a specific control mode, DC bus voltage deviations in the case of a pre-fault rectifier state tends to be more serious than in the case of pre-fault inverter state. Moreover, compared with others, the power direction under the AC voltage control mode is prone to convert into inverter state.

3) The proposed method manages to limit the overcurrent of BIC by regulating the predicted references in abc frame for thermal limitations, and adjust in the positive and negative sequence dq frame to limit the variation/oscillation of DC bus voltage, which can be extended to all three modes of BIC with bidirectional power flow and can effectively improve the quality of BIC current.

REFERENCES

- [1] A. Gupta, S. Doolla, and K. Chatterjee, "Hybrid AC-DC microgrid: systematic evaluation of control strategies," *IEEE Transactions on Smart Grid*, vol. 9, no. 4, pp. 3830–3843, Jul. 2018.
- [2] P. C. Loh, D. Li, Y. K. Chai, and F. Blaabjerg, "Autonomous operation of hybrid microgrid with AC and DC subgrids," *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2214–2223, May 2013.
- [3] S. Mirsaeidi, X. Z. Dong, S. X. Shi, and D. Tzelepis, "Challenges, advances and future directions in protection of hybrid AC/DC microgrids," *IET Renewable Power Generation*, vol. 11, no. 12, pp. 1495–1502, Oct. 2017.
- [4] X. Shen, D. Tan, Z. K. Shuai, and A. Luo, "Control techniques for bidirectional interlinking converters in hybrid microgrids: leveraging the advantages of both AC and DC," *IEEE Power Electronics Magazine*, vol. 6, no. 3, pp. 39–47, Sep. 2019.
- [5] F. Luo, K. H. Loo, and Y. M. Lai, "A hybrid AC/DC microgrid control scheme with voltage-source inverter-controlled interlinking converters," in *Proceedings of the 18th European Conference on Power Electronics and Applications*, Karlsruhe, Germany, 2016, pp. 1–8.
- [6] H. M. Zhao, Z. K. Shuai, J. Ge, A. Luo, W. M. Wu, and Z. J. Shen, "Asymmetrical fault current calculation method and influencing factors analysis of droop-controlled inverter," *CSEE Journal of Power and Energy Systems*, doi: 10.17775/CSEEJPES.2020.05210.
- [7] Z. K. Shuai, C. Shen, X. Yin, X. Liu, and Z. J. Shen, "Fault analysis of inverter-interfaced distributed generators with different control schemes," *IEEE Transactions on Power Delivery*, vol. 33, no. 3, pp. 1223–1235, Jun. 2018.
- [8] A. Sallam, M. E. Nassar, and M. M. A. Salama, "Fault current calculations for interlinked hybrid microgrids," in *Proceedings of 2018 IEEE International Energy Conference*, Limassol, Cyprus, 2018, pp. 1–5.
- [9] L. H. Jia and H. X. Li, "Analysis of AC asymmetrical fault on DC control system in hybrid AC/DC microgrid," in *Proceedings of China International Conference on Electricity Distribution*, Tianjin, China, 2018, pp. 2093–2098.
- [10] L. Meegahapola, I. U. Nutkani, and B. McGrath, "Investigation of fault ride-through capability of AC/DC hybrid microgrids during AC network faults," in *Proceedings of 2017 IEEE Power & Energy Society General Meeting*, Chicago, USA, 2017, pp. 1–5.
- [11] J. Ge, Z. K. Shuai, C. M. Tu, A. Luo, and Z. J. Shen, "Flexible control strategy for enhancing power injection capability of three-phase four-wire inverter during asymmetrical grid faults," *IEEE Transactions on Power Electronics*, vol. 36, no. 8, pp. 9592–9608, Aug. 2021.
- [12] Y. H. Xia and T. Long, "Chopperless fault ride-through control for DC microgrids," *IEEE Transactions on Smart Grid*, vol. 12, no. 2, pp. 965–976, Mar. 2021.
- [13] Z. K. Shuai, W. Huang, C. Shen, J. Ge, and Z. J. Shen, "Characteristics and restraining method of fast transient inrush fault currents in synchronverters," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 9, pp. 7487–7497, Sep. 2017.
- [14] P. Piya, M. Ebrahimi, M. Karimi-Ghartemani, and S. A. Khajehoddin, "Fault ride-through capability of voltage-controlled inverters," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 10, pp. 7933–7943, Oct. 2018.
- [15] X. C. Lin, Z. G. Liang, Y. Zheng, Y. B. Lin, and Y. Kang, "A current limiting strategy with parallel virtual impedance for three-phase three-leg inverter under asymmetrical short-circuit fault to improve the

controllable capability of fault currents,” *IEEE Transactions on Power Electronics*, vol. 34, no. 8, pp. 8138–8149, Aug. 2019.

- [16] C. Shen, Z. K. Shuai, Y. Shen, Y. L. Peng, X. Liu, Z. Y. Li, and Z. J. Shen, “Transient stability and current injection design of paralleled current-controlled VSCs and virtual synchronous generators,” *IEEE Transactions on Smart Grid*, vol. 12, no. 2, pp. 1118–1134, Mar. 2021.
- [17] N. Bottrell and T. C. Green, “Comparison of current-limiting strategies during fault ride-through of inverters to prevent latch-up and wind-up,” *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3786–3797, Jul. 2014.
- [18] B. Mahamedi, M. Eskandari, J. E. Fletcher, and J. G. Zhu, “Sequence-based control strategy with current limiting for the fault ride-through of inverter-interfaced distributed generators,” *IEEE Transactions on Sustainable Energy*, vol. 11, no. 1, pp. 165–174, Jan. 2020.
- [19] W. Pei, X. Zhang, W. Deng, C. Tang and L. Yao, “Review of Operational Control Strategy for DC Microgrids with Electric-hydrogen Hybrid Storage Systems,” *CSEE Journal of Power and Energy Systems*, vol. 8, no. 2, pp. 329–346, Mar. 2022.
- [20] W. H. Wu, Y. D. Chen, A. Luo, L. M. Zhou, X. P. Zhou, L. Yang, Y. T. Dong, and J. M. Guerrero, “A virtual inertia control strategy for DC microgrids analogized with virtual synchronous machines,” *IEEE Transactions on Industrial Electronics*, vol. 64, no. 7, pp. 6005–6016, Jul. 2017.
- [21] Z. Liu, S. Miao, W. Wang and D. Sun, “Comprehensive control scheme for an interlinking converter in a hybrid AC/DC microgrid,” *CSEE Journal of Power and Energy Systems*, vol. 7, no. 4, pp. 719–729, Jul. 2021.
- [22] F. R. Xiao, L. Dong, L. Li, and X. Z. Liao, “A frequency-fixed SOGI-based PLL for single-phase grid-connected converters,” *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 1713–1719, Mar. 2017.
- [23] A. Kumar, M. Rizwan and U. Nangia, “A New Approach to Design and Optimize Sizing of Hybrid Microgrids in Deregulated Electricity Environment,” *CSEE Journal of Power and Energy Systems*, vol. 8, no. 2, pp. 569–579, Mar. 2022.



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